REMARKS

By this Amendment, claim 1 is amended to merely clarify the recited subject matter and new claim 5 is added to more fully claim the disclosed invention (patentable for the same reasons asserted herein with regard to the rejected claims). Claims 1-5 are pending.

Claims 1-4 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (U.S. 2002/0173173; hereafter "Kobayashi"). Applicants traverse the rejection because Kobayashi fails to disclose, teach or suggest all the features recited in the rejected claims. For example, Kobayashi fails to disclose, teach or suggest the claimed invention including The method for eliminating boron contamination in an annealed wafer, the method including annealing a silicon wafer having a surface on which a native oxide film has formed containing boron of environmental origin or from chemical treatment prior to the annealing, wherein, in the annealing, the silicon wafer is subjected to temperature heat-up in a mixed gas atmosphere having a ratio of hydrogen gas to an inert gas of 5% to 100% so as to remove the boron-containing native oxide film, and subsequent annealing in an inert gas atmosphere, wherein a boron concentration in the wafer surface and a boron concentration in the bulk silicon are made to be substantially same by the annealing, as recited in independent claim 1 and its dependent claims 2-5.

Kobayashi merely teaches an annealed wafer manufacturing method that uses a heat treatment method causing no change in resistivity of a wafer surface even when a silicon wafer is subjected to heat treatment in an inert gas atmosphere. Kobayashi's manufacturing method enables heat treatment in an ordinary diffusion furnace not requiring any specific facility. As a result of the manufacturing process, an annealed wafer is provided in which a boron concentration in the vicinity of a surface thereof is constant and crystal defects are annihilated (paragraph (0013) of Kobayashi).

In Kobayashi's method, a silicon wafer is subjected to heat treatment in an atmosphere containing hydrogen gas; thereby, the deposited boron is removed before the natural oxide film is removed. The Boron deposited on the surface of the wafer hardly diffuses into the wafer when a natural oxide film is present on the wafer surface. Therefore, before removing the natural oxide film, the deposited boron is removed using hydrogen gas in a state where the natural oxide film is present. As a result, Kobayashi prevents a resistivity change in the vicinity of the wafer surface due to the diffusion of boron into the wafer (paragraph (0015) of Kobayashi).

Kobayashi teaches use of a hydrogen concentration in the range from 0.1% or more to a lower explosion limit (4%) or less. Thus, Kobayashi teaches that, by controlling the hydrogen concentration to be the lower explosion limit (4%) or less, it is possible to use an ordinary diffusion furnace for the heat treatment without requiring any specific facility. Kobayashi further teaches that the natural oxide film is removed by the heat treatment in an inert gas atmosphere.

However, Kobayashi fails to teach or suggest controlling a ratio of hydrogen gas to an inert gas to be 5% to 100%, so as to remove a native oxide film and its effect of removing the boron in the surface and in the oxide film.

Further, Kobayashi fails to teach or suggest removing the entire oxide film by annealing, thereby removing the boron in the surface and in the oxide film. As explained in Applicants' specification, differences in boron concentration do not arise between the surface of the resulting annealed wafer and the silicon bulk. Thus, the electrical characteristics in the wafer surface do not change, making it possible to reliably and effectively prevent a decline in the manufacturing yield of semiconductor devices (page 8, lines 17 to 20).

Moreover, Kobayashi fails to teach or suggest the claimed invention wherein the boron concentration in the wafer surface and the boron concentration in bulk silicon are substantially same; rather, Kobayashi's express aim is to maintain the wafer's boron concentration in the vicinity of a surface thereof as constant. Therefore, Kobayashi actually teaches away from the claimed invention.

Accordingly, Applicants submit that the claimed invention is patentable over the teachings of Kobayashi because Kobayashi fails to teach or suggest the claimed method for eliminating boron contamination in an annealed wafer, the method including annealing a silicon wafer having a surface on which a native oxide film has formed containing boron of environmental origin or from chemical treatment prior to the annealing, wherein, in the annealing, the silicon wafer is subjected to temperature heat-up in a mixed gas atmosphere having a ratio of hydrogen gas to an inert gas of 5% to 100% so as to remove the boron-containing native oxide film, and subsequent annealing in an inert gas atmosphere, wherein a boron concentration in the wafer surface and a boron concentration in the bulk silicon are made to be substantially same by the annealing, as recited in independent claim 1 and its dependent claims 2-5.

Thus, Applicants request issuance of a Notice of Allowability for all pending claims. However, if anything is necessary to place the application in condition for allowance, Applicant requests that the Examiner telephone the undersigned Applicant representative.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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